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REISSUE PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	96-C-126RE (1678-31)
First Named Inventor	Frank Randolph Bryant
Original Patent Number	5,825,070
Original Patent Issue Date (Month/Day/Year)	10/20/98
Express Mail Label No.	EJ754983690US

APPLICATION FOR REISSUE OF: *(check applicable box)* ☒ *Utility Patent* ☐ *Design Patent* ☐ *Plant Patent*

APPLICATION ELEMENTS (37 CFR 1.173)	ACCOMPANYING APPLICATION PARTS
1. ☐ * Fee Transmittal Form *(e.g., PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*	7. ☐ Statement of status/support for all changes to the claims. See 37 CFR 1.173(c).
2. ☐ Applicant claims small entity status See 37 CFR 1.27.	8. ☐ Original U.S. Patent for surrender ☐ Ribboned Original Patent Grant ☐ Statement of Loss (PTO/SB/55)
3. ☒ Specification and Claims in a double column copy of patent format *(amended, if appropriate)*	9. ☐ Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
4. ☒ Drawing(s) *(proposed amendments, if appropriate)*	10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
5. ☒ Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*	11. ☐ English Translation of Reissue Oath/Declaration *(if applicable)*
6. Original U.S. Patent currently assigned? ☒ Yes ☐ No *(If Yes, check applicable box(es))* ☐ Written Consent of all Assignees *(PTO/SB/53)* ☒ 37 C F.R. § 3.73(b) Statement (PTO/SB/96) ☐ Power of Attorney	12. ☒ Preliminary Amendment 13. ☒ Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)* 14. ☒ Other: Assent of Assignee; Certificate of Express Mailing

14. CORRESPONDENCE ADDRESS

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Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicants: Frank Randolph Bryant and Tsiu Chiu Chan

Reissue Application No.: Filed: October 20, 2000

For: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

STMicroelectronics, Inc., a corporaton
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, government agency, etc.)

certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from inventor of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____ Frame _____ (copy enclosed).

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignees as shown below:

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[ ] Additional documents in the chain of title are listed on a supplemental sheet.

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The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: _____

Name: Lisa K. Jorgenson

Title: Director of Intellectual Property & Assistant Secretary

Signature:_____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: Frank Randolph Bryant
Tsiu Chiu Chan

Patent No.: 5,825,070

Title: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

Issued: October 20, 1998

Atty Dk No.: 96-C-126

Reissue Application

Applicants: Frank Randolph Bryant
Tsiu Chiu Chan

Serial No.:

Title: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

Filing Date: October 20, 2000

Atty Dk No.: 96-C-126RE (1678-31)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EJ754983690US

Date of Deposit: October 20, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR, Section 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box PATENT APPLICATION, Washington, D.C. 20231 by

Kelly Pedersen
Signature

ASSENT OF ASSIGNEE

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

STMicroelectronics, Inc. (formerly known as SGS-Thomson Microelectronics, Inc.), assignee of U.S. Patent No. 5,825,070, consents to the filing of reissue application No. ________________ or the present application, if filed with the initial application papers) for the reissue of U.S. Patent No. 5,825,070.

STMicroelectronics, Inc.

____

Lisa K. Jorgenson
Director of Intellectual Property
Assistant Secretary

United States Patent [19]

Bryant et al.

[54] **STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL**

[75] Inventors: **Frank Randolph Bryant**, Denton; **Tsiu Chiu Chan**, Carrollton, both of Tex.

[73] Assignee: **STMicroelectronics, Inc.**, Carrollton, Tex.

[21] Appl. No.: **712,808**

[22] Filed: **Sep. 12, 1996**

Related U.S. Application Data

[60] Continuation-in-part of Ser. No. 390,117, Feb. 17, 1995, abandoned, which is a division of Ser. No. 159,462, Nov. 30, 1993, Pat. No. 5,426,065.

[51] **Int. Cl.**[6] **H01L 29/76**; H01L 29/94; H01L 31/062

[52] **U.S. Cl.** **257/392**; 257/379; 257/903; 257/904

[58] **Field of Search** 257/903, 904, 257/368, 379, 392

[56] **References Cited**

U.S. PATENT DOCUMENTS

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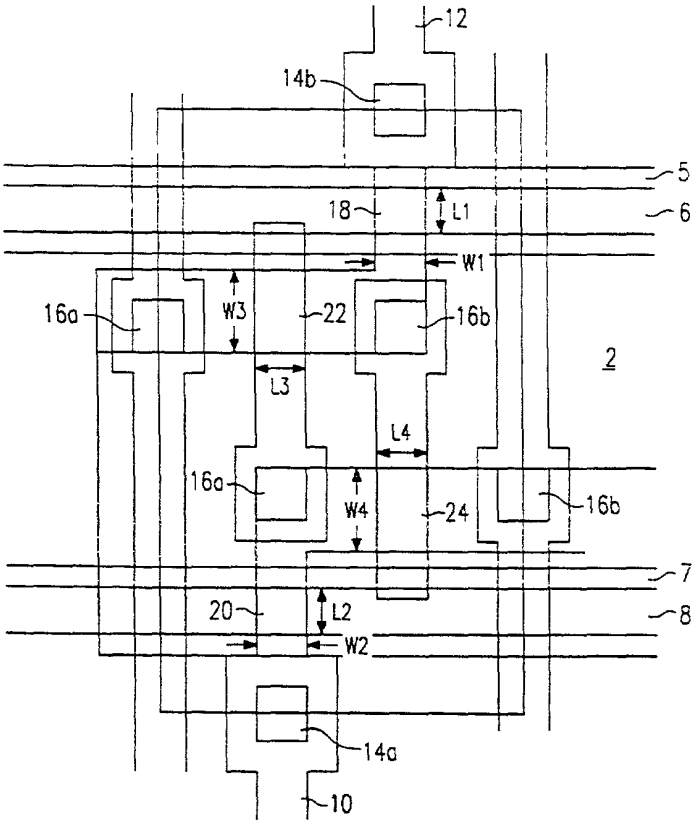

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[11] **Patent Number: 5,825,070**

[45] **Date of Patent: Oct. 20, 1998**

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5,373,170 12/1994 Pfiester et al. 257/69

Primary Examiner—Ngân V. Ngô
Attorney, Agent, or Firm—Theodore E. Galanthay; Kenneth C. Hill; Lisa K. Jorgenson

[57] ABSTRACT

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein and the first thickness is different from the second thickness.

12 Claims, 7 Drawing Sheets

STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation in part of an application entitled "METHOD OF MAKING TRANSISTOR DEVICES IN AN SRAM CELL", Ser. No. 08/390,117, filing date Feb. 17, 1995, which is a divisional of Ser. No. 08/159,462 filed Nov. 30, 1993, now U.S. Pat. No. 5,426,065.

Applicant incorporates said application Ser. No. 08/159,462 by reference herein and claims the benefit of said application for all purposes pursuant to 37 C. F. R. § 1.78.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated the circuit devices and more specifically to field effect transistors (FET) for use in integrated circuits.

2. Description of the Prior Art

Memories are devices that respond to operational orders, usually from a central processing unit. Memories may store large quantities of information in a digital format. In a memory system or unit, addresses are used to access the contents of the memory unit. A binary digit, also called a bit, is the basic information element stored in a memory unit. The smallest subdivision of a memory unit into which a bit of information can be stored is called a memory cell. A memory on a chip is physically arranged as a two-dimensional array of cells, wherein rows of cells are connected by row lines, also called word lines. A column of cells are connected by a column line, also called a bit line. These memory cells may be constructed by various configurations of transistors and/or capacitors.

A semiconductor memory is a memory that is implemented in a semiconductor material such as silicon. Metal-oxide semiconductor (MOS) memories are common in the industry. A number of different types of MOS memories exist, such as a dynamic random access memory (DRAM) which is a metal oxide semiconductor memory that stores a bit of information as a charge on a capacitor, and a static random access memory (SRAM) which includes a bistable flipflop circuit requiring only a DC voltage applied to it to retain its memory. Normally, an SRAM contains four transistors plus either two transistors or two polysilicon load resistors as pull-up devices.

SRAMs have a disadvantage over a memory such as a DRAM. The components in an SRAM typically require the SRAM to have a larger basic cell than a DRAM. In SRAM memory cells, the data transfer gate transistor to pull-down transistor ON resistance ratio is typically required to be about 2.6× or greater to provide stability to the memory cell. Currently, the width of the pull-down transistor is required to be larger than the width of the transfer gate transistor to achieve the ratio requirement. This requirement places limitations on how small the memory cell may be made. Therefore, it would be desirable to have a transistor structure that would allow for a reduction in the area that a memory cell requires.

SUMMARY OF THE INVENTION

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second

transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein the first thickness is different from the second thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic diagram of an SRAM cell in which a preferred embodiment of a present invention may be implemented;

FIG. 2 is a layout of the SRAM cell depicted in FIG. 1;

FIGS. 3A–3E are schematic cross-section views of a transfer gate transistor and pull-down transistor in an SRAM cell during processing; and

FIGS. 4–13 are layout diagrams of an SRAM during processing according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections and layouts of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

FIG. 1 is a schematic diagram of an SRAM cell 2 in which a preferred embodiment of the present invention may be implemented. SRAM cell 2 includes transistors TG1, TG2, PD1, and PD2. SRAM cell 2 also includes resistors R1 and R2. Transistors TG1 and TG2 are transfer gate transistors in SRAM cell 2 while transistors PD1 and PD2 are pull-down transistors. Resistors R1 and R2 are used as pull-up devices.

Transistor TG1 has a source/drain connected to bit line A, and transistor TG2 has a source/drain connected to bit line B. Bit line B is a complement of bit line A. The gates of transistors TG1 and TG2 are connected to word line C. As can be seen, transistors PD1 and PD2 are connected in a cross-coupled configuration. In addition, the source/drain of transistor TG1 and transistor PD1 is connected to one end of resistor R1 while the source/drain of transistor PD2 and transistor TG2 are connected to one end of resistor R2. The other ends of resistors R1 and R2 are connected to power

supply voltage VCC while transistors PD1 and PD2 each have a source/drain connected to power supply voltage VSS.

Typically, the power supply voltage VCC is at a higher voltage than power supply voltage VSS. In a typical SRAM cell, transistors PD1 and PD2 typically have a width of 2.1μ and a length of 0.7μ. Transistors PG1 and PG2 typically have a width of 0.9μ and a length of 0.8μ.

Referring now to FIG. **2**, a layout of SRAM cell **2** from FIG. **1** is depicted. SRAM cell **2** in FIG. **2** includes word lines **6** and **8**, which are poly 1 lines. Bit lines **10** and **12** include bit line contacts **14***a* and **14***b*. In addition, SRAM cell 2 also has shared contacts **16***a* and **16***b*. Transistor TG1 includes a gate **18**. Transistor TG1 has a width W1 and a length L1. Similarly, transistor TG2 has a gate **20** and a width W2 and a length L2. Pull-down transistor PD1 includes gate **22** and has a width W3 and a length L3; pull-down transistor PD2 includes gate **24** and has a width W4 and a length L4.

FIGS. 3A–3E are cross-section views of a transfer gate transistor and a pull-down transistor according to the present invention. Specifically, FIG. 3A is a cross-section view of a pull-down transistor **26**, which includes a substrate **30** that is typically a monocrystalline silicon of a conventional crystal orientation known in the art. Many features of the present invention are applicable to devices employing semiconductor materials other than silicon as will be appreciated by those of ordinary skill in the art. Substrate **30** may be either a p-type substrate or an n-type substrate. In the present illustrative example, a p-type substrate is employed.

As can be seen in FIG. 3A, a gate structure has been formed, which includes gate oxide layer **32** and polysilicon layer **34**. Source drain regions **36** have been implanted into substrate **30**. Various types of implants may be employed; for example, n-type impurities may be implanted into a p-type substrate. Source drain regions **36** are n-type active regions in the illustrated example. Lightly doped drain (LDD) regions **38** are defined using sidewall oxide spacers **40** as known by those skilled in the art. Alternatively, LDDs **38** and sidewall spacers **40** may be omitted.

Transfer gate transistor **28** in FIG. 3B is at the same processing step as pull-down transistor **26** in FIG. 3A. After formation of the gate oxide **32** in FIG. 3A, the region in which transfer gate transistor **28** is to be formed is masked off. Thus, no processing is performed in the region of transfer gate transistor **28** while the rest of pull-down transistor **26** is formed. As can be seen in this portion of SRAM cell **4**, a window **42** has been opened in dielectric layer **44** exposing gate oxide layer **32**. Dielectric layer **44** is an oxide in this example. Next, gate oxide layer **32** is etched away in FIG. 3C, exposing surface **46** of substrate **30**. Thereafter, a new gate oxide layer **48** is grown on surface **46** of substrate **30** in window **42**, as shown in FIG. 3D. This new gate oxide layer **48** preferably has a thickness less than that of the original gate oxide layer **32**.

Thereafter, the gate of pull-down transistor **28** is formed as illustrated in FIG. 3E. The gate of pull-down transistor **28** includes gate oxide layer **48** and polysilicon layer **50**. Source/drains **52** also are implanted in substrate **30**. Source/drains **52** include LDDs **54**, which are again defined using sidewall oxide spacers **56**. The thickness of gate oxide **32** is greater than the thickness of gate oxide **48**. This type of processing is employed to create transfer gate transistors and pull-down transistors with different gate oxide thicknesses, which allows for a reduction in the width of pull-down transistors in an SRAM cell.

Although the depicted embodiment illustrates completely etching away the gate oxide of pull-down transistor **28**, then

producing a gate oxide of the desired thickness, other methods of producing different gate oxides may be employed according to the present invention. For example, a gate oxide layer may be grown for transfer gate transistor **28** first, and then an additional gate oxide layer can be grown on both pull-down transistor **26** and transfer gate transistor **28** to produce gate oxide layers of different thicknesses for each of the transistors. Transfer gate transistor **28** is completely masked from processing after completion, and remains in the form depicted in FIG. **3**A during the various processing steps applied to pull-down transistor **28** in FIGS. **3**B–**3**C.

According to the present invention, a reduced width pull-down transistor dimension may be employed by adjusting the ratio of the gate oxide thickness between the transfer gate transistors and the pull-down transistors in the SRAM cell. The needed thicknesses of the two gate oxides may be selected using the following equation:

$$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \quad \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \quad \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistor and the pull-down transistor, TOX_{tg} is the gate oxide thickness of the transfer gate transistor, TOX_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is the width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vcc is the upper power supply voltage, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

In the depicted example, RATIO is 2.6, VCC is equal to 3.3 volts, Vt_{tg} is 0.9 volts with a back bias, and Vt_{pd} is equal to 0.7 volts. If 0.5μ feature design rules are utilized (L equal 0.5μ, W equal 0.6μ), the pull-down transistor width is 1.56μ. If the pull-down gate oxide thickness is 120 Å, a 36% reduction in pull-down transistor width (1.0μ feature), will require a 134 Å transfer gate oxide thickness. A 50% reduction in pull-down transistor width (0.8μ feature) requires a 165 Å transfer gate oxide thickness. By reducing the width (W_{pd}) of the pull-down transistor, the overall area of SRAM cell may be reduced.

FIGS. **4**–**13** are layout diagrams of an SRAM cell during processing according to the present invention. In FIG. **4**, SRAM cell **4** located on a wafer has been processed and is ready for gate oxide. Active areas **100** have been formed in the substrate of the wafer by growing a field oxide everywhere else. Transfer gate oxide is grown on the wafer and a poly **1** is deposited. In FIG. **5**, the poly **1** is patterned for transfer gate transistors in areas **102**. Drain/source implantation for the transfer gate transistors is performed with resist patterns blocking implant into pull-down transistor areas **104** in FIG. **6**. Thereafter, a blanket threshold voltage adjust implant is performed for the pull-down transistors. Then undoped oxide is deposited on the wafer in a thickness of about 1000 Å. The undoped oxide is removed in FIG. **7**. Undoped oxide in areas **106** are protected from removal with resist patterns to protect the poly **1**, which causes only those areas **104** intended for the pull-down transistors to be exposed. The pull-down transistor gate oxide is grown; a thin buffer of poly is deposited in a layer of about 500 Å. In FIG. **8**, resist patterns are utilized to open shared contacts in areas **108**. Then, poly plus polycide is deposited for poly **2**.

In FIG. **9**, the poly **2** is patterned for pull-down transistors and the Vss line as shown in areas **110** in FIG. **9**. Drain/source implantation is then performed for the pull-down

transistors. Thereafter, a thin oxide is deposited over the wafer in a layer of about 700 Å. A spin-on-glass process is performed to create a glass layer of about 700 Å. This layer is cured and densified. Thereafter, thin glass is deposited on the wafer in a layer of about 700 Å. In FIG. 10, second shared contacts are opened using resist patterns to protect the rest of the SRAM cell from being opened. The second shared contacts are opened in areas 112. Then, undoped poly 3 is deposited in a layer of about 700 Å thick. In FIG. 11, the poly 3 is patterned with resist to remain in areas 114. This poly layer will be used for the SRAM cell pull-up resistors, and VCC supply lines. Undoped oxide is deposited in a layer of about 1000 Å on the wafer and a blanket implant for poly 3 is performed to set the poly resistor resistance on the wafer. Thereafter, a n+ implant is performed for the VCC portions of poly 3 utilizing a resist pattern covering areas 116 in FIG. 12. Contact windows are cut in areas 118 in FIG. 13.

Thus, the present invention provides a method and structure for reducing the overall cell area of a memory cell. The present invention provides an ability to reduce the area of a memory cell by allowing the widths of the pull-down transistors to be reduced. The reduction in width is accomplished according to the present invention by selecting different gate oxide thicknesses for the pull-down transistor and the transfer gate transistor to maintain the desired ratio.

Although the depicted embodiment defines specific numbers for ratios, widths, lengths, in other parameters may be utilized by those of ordinary skill in the art following this disclosure. In addition, the different gate oxide thicknesses for transistors in the SRAM memory cell may be applied to other types of memory cells in which widths or lengths of transistors can affect the area that a cell requires.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. An SRAM memory cell comprising:

a first and second transfer gate transistors, the first transfer gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; and

first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/drain of said first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate transistor, both first and second pull-down transistors having a second source/drain connected to a power supply voltage node;

wherein the first and second transfer gate transistors each have a first width and include a gate oxide layer having a first thickness, the first and second pull-down transistors each have a second width and include a gate oxide layer having a second thickness, and a product of the first width and the first thickness is greater than or equal to a product of the second width and the second thickness.

2. The SRAM memory cell of claim 1, wherein the first thickness is thicker than the second thickness.

3. The SRAM memory cell of claim 2, wherein the first thickness is greater than two times the second thickness.

4. The SRAM memory cell of claim 1, wherein the first and second thicknesses are determined as follows:

$$\text{RATIO} \leqq \frac{Tox_{tg}}{Tox_{pd}} \quad \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \quad \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

5. The SRAM memory cell of claim 4, wherein RATIO is equal to 2.6.

6. A semiconductor circuit comprising:

a first transistor having a first width and a first gate including a gate oxide layer having a first thickness; and

a second transistor having a second width and a second gate including a gate oxide layer having a second thickness, wherein a product of the second width and the second thickness is greater than a product of the first width and the first thickness.

7. The semiconductor circuit of claim 6, wherein the first transistor is a pull-down transistor in an SRAM memory cell.

8. The semiconductor circuit of claim 7, wherein the second transistor is a transfer gate transistor in the SRAM memory cell.

9. The semiconductor circuit of claim 8, wherein the gate oxide thickness of the pull-down transistor and a transfer gate transistor in the SRAM memory cell are selected using the following:

$$\text{RATIO} \leqq \frac{Tox_{tg}}{Tox_{pd}} \quad \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \quad \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

10. The semiconductor circuit of claim 9, wherein RATIO is at least 2.6.

11. The semiconductor circuit of claim 10, wherein the pull-down transistor is an n-channel field effect devices.

12. The semiconductor circuit of claim 10, wherein the transfer gate transistor is an n-channel field effect device.

* * * * *

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: Frank Randolph Bryant
Tsiu Chiu Chan

Patent No.: 5,825,070

Title: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

Issued: October 20, 1998

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CERTIFICATE OF MAILING OR TRANSMISSION

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Date of Deposit: October 20, 2000

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Kelly Pedersen
Signature

FIRST PRELIMINARY AMENDMENT

October 20, 2000

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

Please transfer FIGS. 1 – 2, 3B – 3D, and 4 – 13 from the file of the issued `070 patent to the reissue file.

Please amend FIGS. 3A and 3E as requested in the enclosed Request for Drawing Change.

In the Specification:

In Column 3, line 6, please replace "PG1 and PG2" with –[PG1 and PG2] TG1 and TG2--.

In Column 4, please replace with "$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}$" with

$$[\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}]$$

$$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \times \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \times \frac{Vcc - Vtpd}{Vcc - Vt_{tg}}$$

In the Claims:

Please amend the claims as follows:

1. An SRAM memory cell comprising:

[a] first and second transfer gate transistors, the first transfer gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; [and]

first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/ drain of said first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate

transistor, both first and second pull-down transistors having a second source/drain connected to a power supply voltage node; and

wherein the first and second transfer gate transistors each have a first width and include a gate oxide layer having a first thickness, the first and second pull-down transistors each have a second width and include a gate oxide layer having a second thickness, and a product of the [first] second width and the first thickness is greater than or equal to a product of the [second] first width and the second thickness.

4. The SRAM memory cell of claim 1, wherein the first and second thicknesses are determined as follows:

$$[\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}]$$

$$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} x \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} x \frac{Vcc - Vt_{pd}}{Vcc - Vt_{tg}}$$

---

where RATIO is the desired ratio of the transfer gate transistors and the pull down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

6. A semiconductor circuit comprising:

a first transistor having a first width an a first gate including a gate oxide layer having a first thickness; and

a second transistor having a second width and a second gate including a gate oxide layer having a second thickness, wherein a product of the [second] first width and the second thickness is greater than a product of the [first] second width and the first thickness.

9. The semiconductor circuit of claim 8, wherein the gate oxide thickness of the pull-down transistor and a transfer gate transistor in the SRAM memory cell are selected using the following:

$$[\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \; \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \; \frac{Vcc - Vt_{tg}}{Vcc - Vt_{pd}}]$$

$$\text{RATIO} \leq \frac{Tox_{tg}}{Tox_{pd}} \; x \; \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \; x \; \frac{Vcc - Vt_{pd}}{Vcc - Vt_{tg}}$$

---

where RATIO is the desired ratio of the transfer gate transistors and the pull down transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

Please add the following new claims:

13. A semiconductor circuit, comprising:

a first transistor including a first gate having a first width and including a first gate insulator having a first thickness; and

a second transistor including a second gate having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

14. The semiconductor circuit of claim 13 wherein the first transistor comprises a pull-down transistor.

15. The semiconductor circuit of claim 13 wherein the second transistor comprises a transfer gate transistor.

16. The semiconductor circuit of claim 13 wherein the product of the first width and the second thickness is greater than the product of the second width and the first thickness.

17. A semiconductor circuit, comprising:

a first transistor including a first channel region having a first width and including a first gate insulator having a first thickness; and

a second transistor including a second channel region having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

18. The semiconductor circuit of claim 17 wherein the first transistor comprises a pull-down transistor.

19. The semiconductor circuit of claim 17 wherein the second transistor comprises a transfer gate transistor.

20. The semiconductor circuit of claim 17 wherein the product of the first width and the second thickness is greater than the product of the second width and the first thickness.

21. A memory cell, comprising:

a pull-down transistor including a first gate having a first width and including a first gate insulator having a first thickness; and

a transfer gate transistor coupled to the pull-down transistor and including a second gate having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

22. A memory cell, comprising:

a pull-down transistor including a first channel region having a first width and including a first gate insulator having a first thickness; and

a transfer gate transistor including a second channel region having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

REMARKS

Claims 1 – 22 are pending in this broadening reissue application.

The Applicants have amended claims 1, 4, 6, and 9 and have added new circuit claims 13 – 20 and new memory-cell claims 21 – 22 to broaden the scope of protection to their invention. The Applicants have also amended the drawings and specification to correct typographical errors.

The Applicants have added no new matter to the reissue application.

In light of the foregoing, original claims 2 – 3, 5, 7 – 8, and 10 - 12 as issued, claims 1, 4, 6, and 9 as amended, and new claims 13 – 22 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he/she is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 20th day of October, 2000.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

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Attorney for Applicants
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155-108th Avenue N.E., Ste 350
Bellevue, WA 98004-5901
(425) 455-5575

Enclosures

US005825070A

United States Patent [19]

Bryant et al.

[11] Patent Number: 5,825,070

[45] Date of Patent: Oct. 20, 1998

[54] STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

[75] Inventors: **Frank Randolph Bryant**, Denton; **Tsiu Chiu Chan**, Carrollton, both of Tex.

[73] Assignee: **STMicroelectronics, Inc.**, Carrollton, Tex.

[21] Appl. No.: **712,808**

[22] Filed: **Sep. 12, 1996**

Related U.S. Application Data

[60] Continuation-in-part of Ser. No. 390,117, Feb. 17, 1995, abandoned, which is a division of Ser. No. 159,462, Nov. 30, 1993, Pat. No. 5,426,065.

[51] **Int. Cl.**[6] **H01L 29/76**; H01L 29/94; H01L 31/062

[52] **U.S. Cl.** **257/392**; 257/379; 257/903; 257/904

[58] **Field of Search** 257/903, 904, 257/368, 379, 392

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,866,002	9/1989	Shizukuisha et al.	437/34
5,285,096	2/1994	Ando et al.	257/379
5,373,170	12/1994	Pfiester et al.	257/69

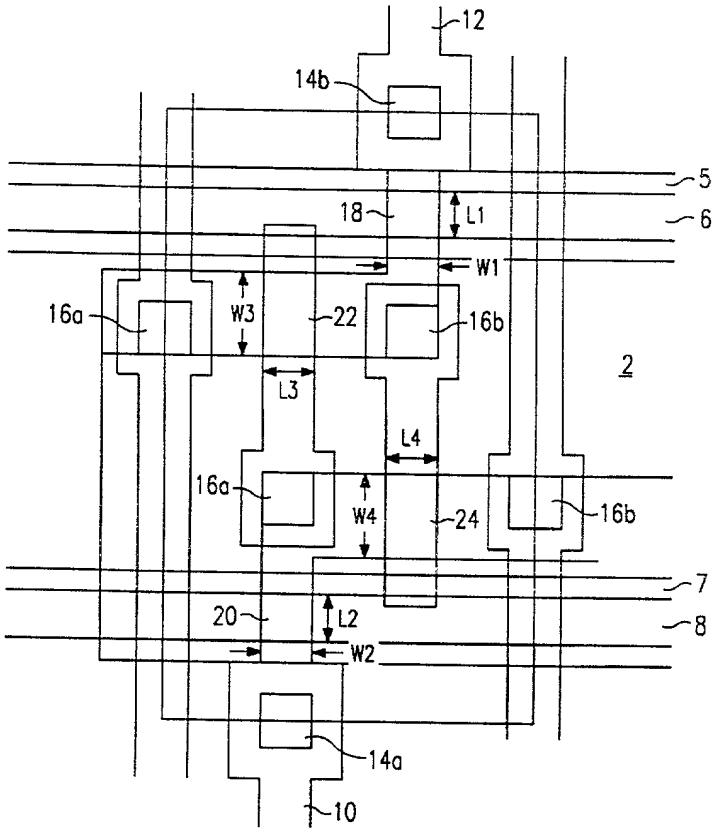
Primary Examiner—Ngân V. Ngô

Attorney, Agent, or Firm—Theodore E. Galanthay; Kenneth C. Hill; Lisa K. Jorgenson

[57] **ABSTRACT**

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein and the first thickness is different from the second thickness.

12 Claims, 7 Drawing Sheets



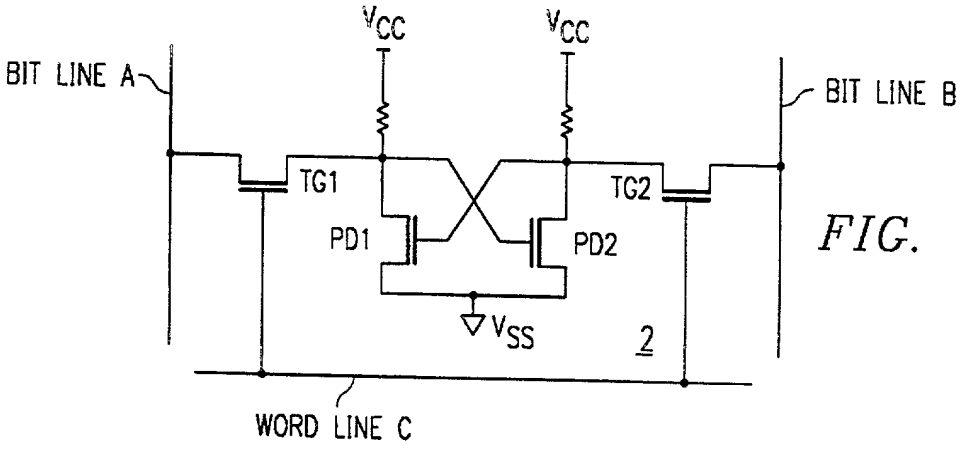

V_{CC}
V_{CC}
BIT LINE A
BIT LINE B
TG1
TG2
PD1
PD2
V_{SS}
2
WORD LINE C

FIG. 1

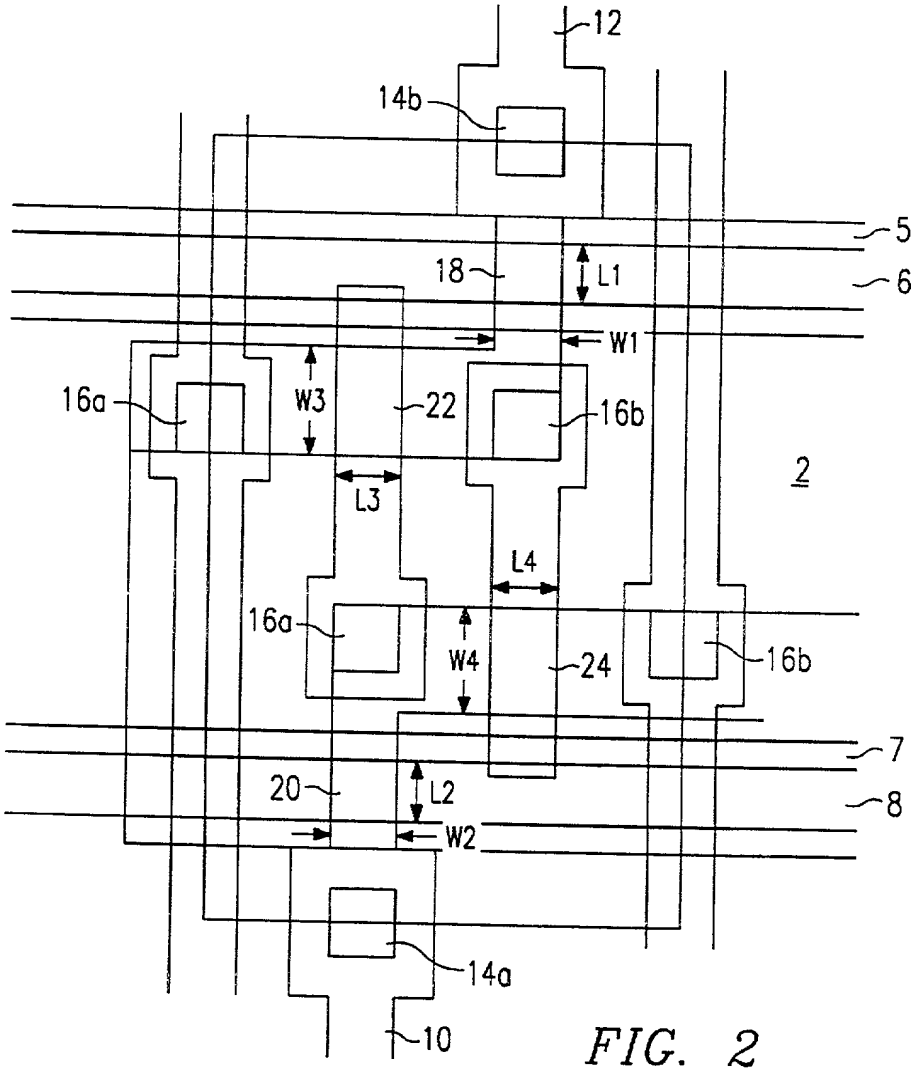

12
14b
5
18
L1
6
W1
W3
16a
22
16b
2
L3
L4
16a
W4
24
16b
7
20
L2
8
W2
14a
10

FIG. 2

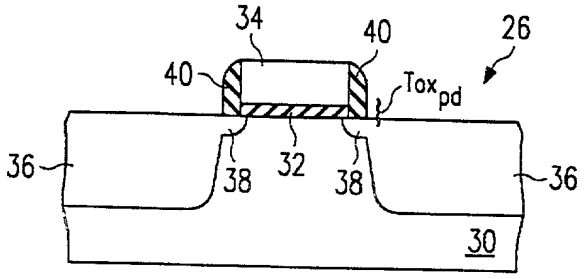


FIG. 3A

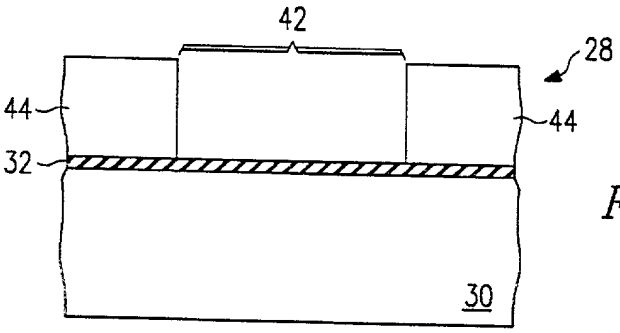


FIG. 3B

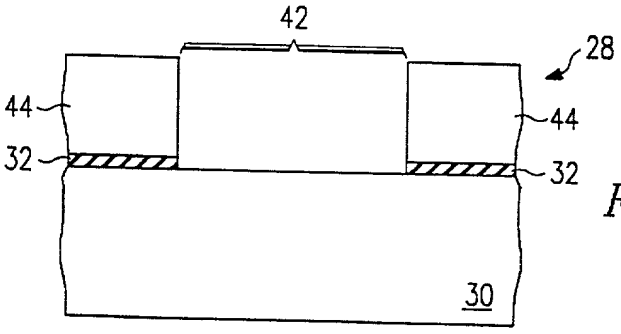


FIG. 3C

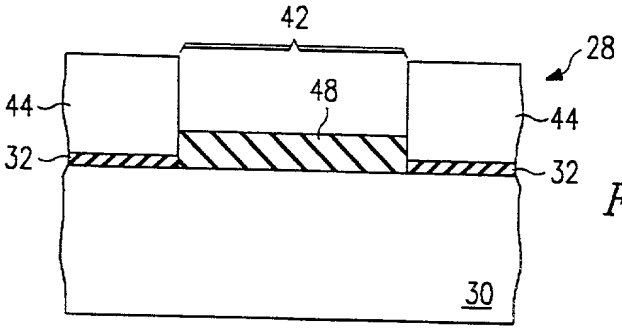


FIG. 3D

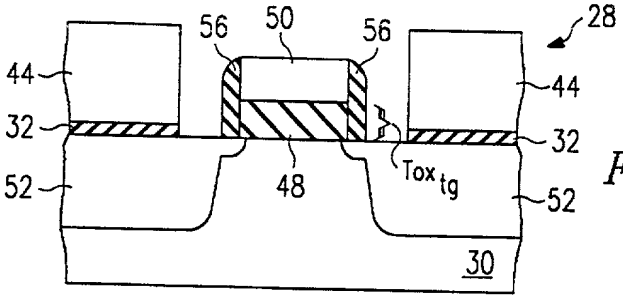


FIG. 3E

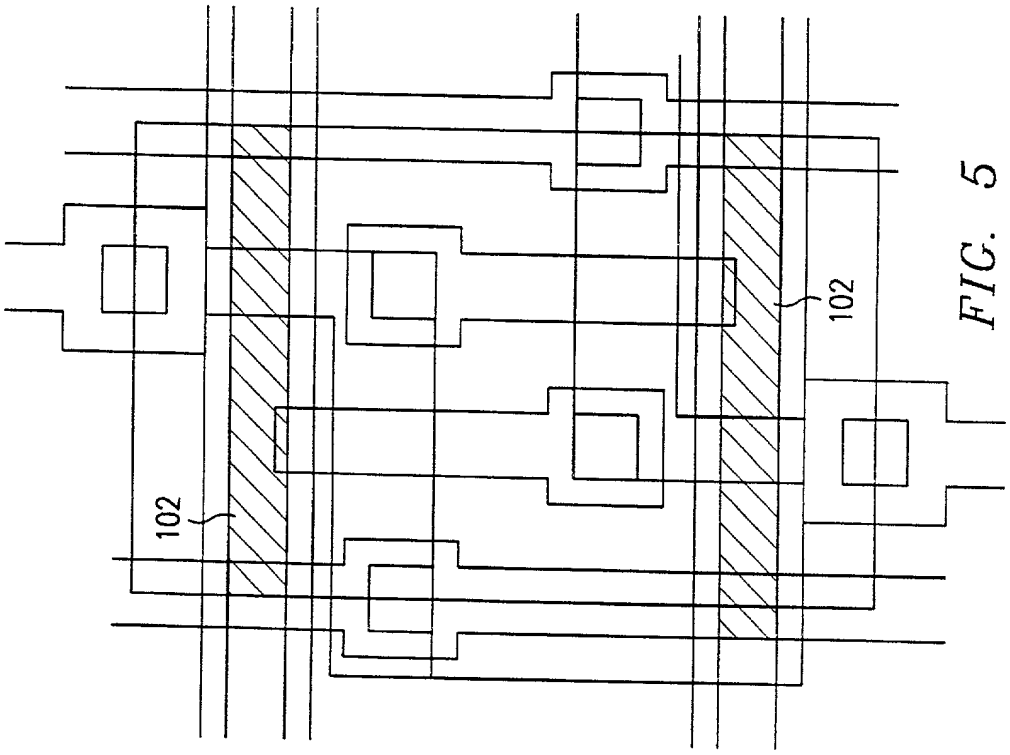


FIG. 5

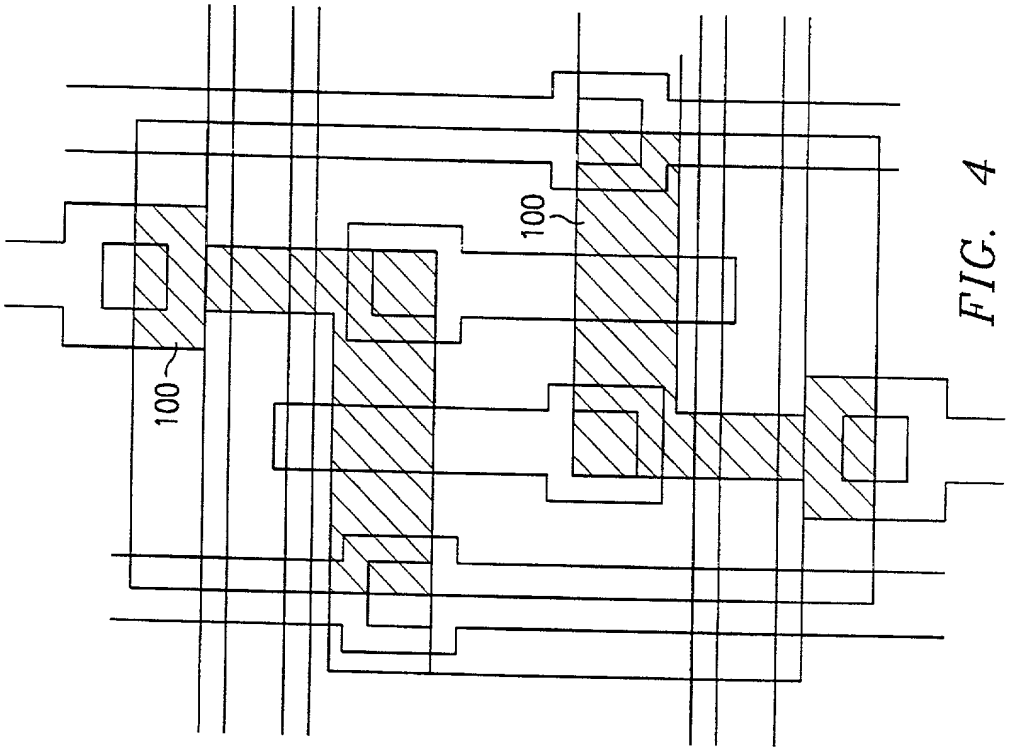


FIG. 4

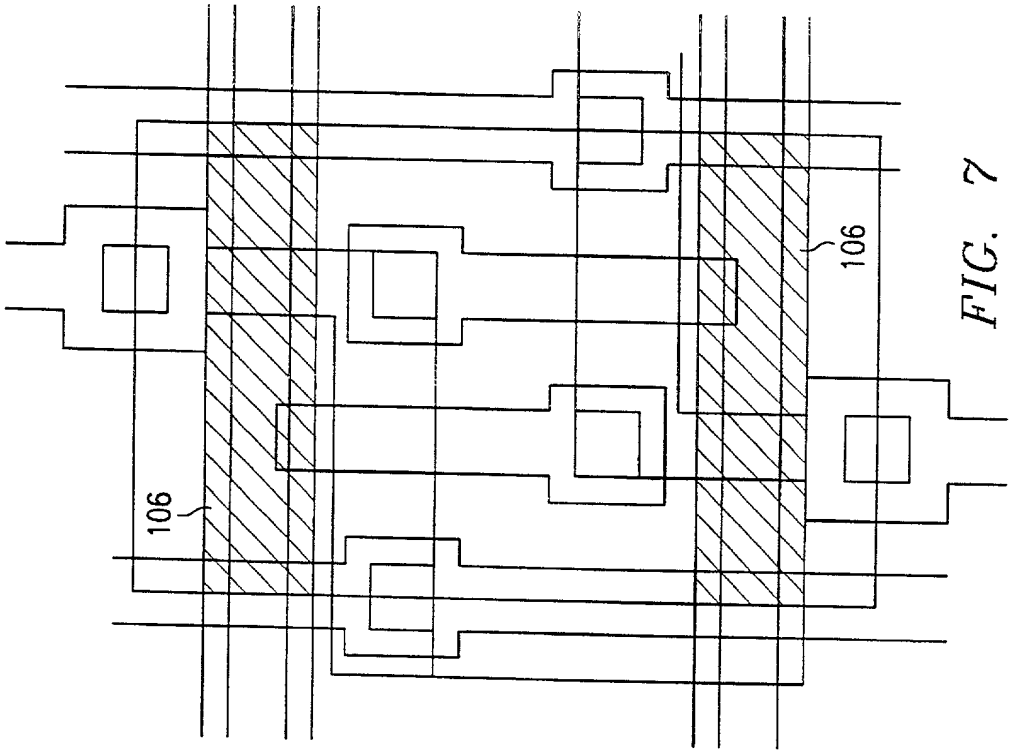


FIG. 7

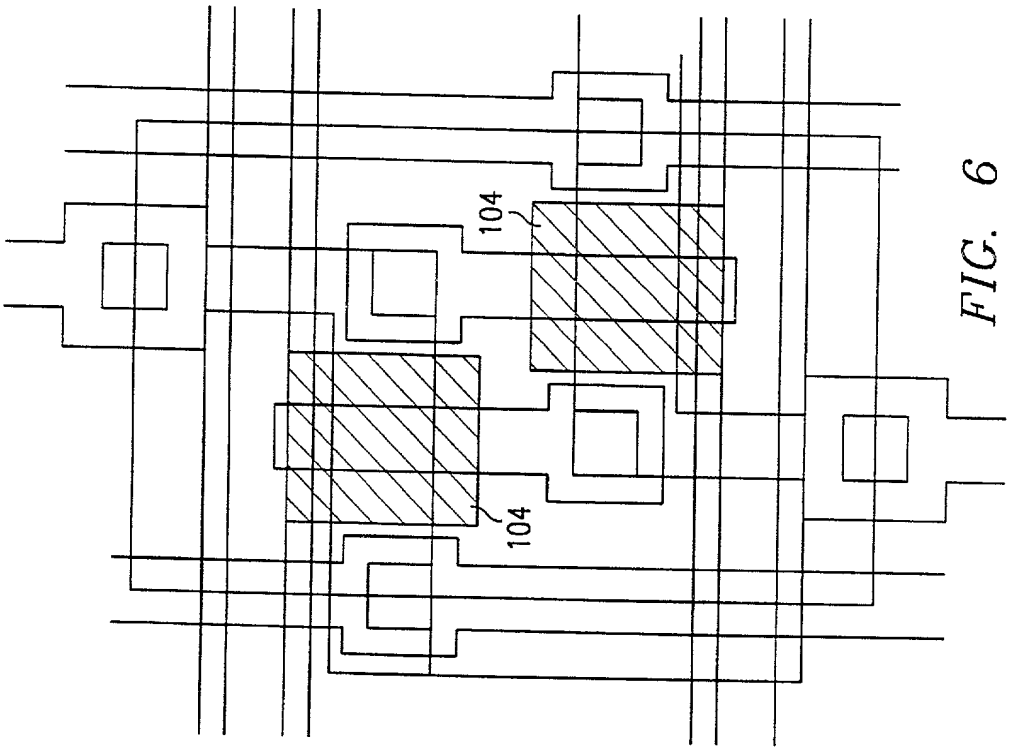


FIG. 6

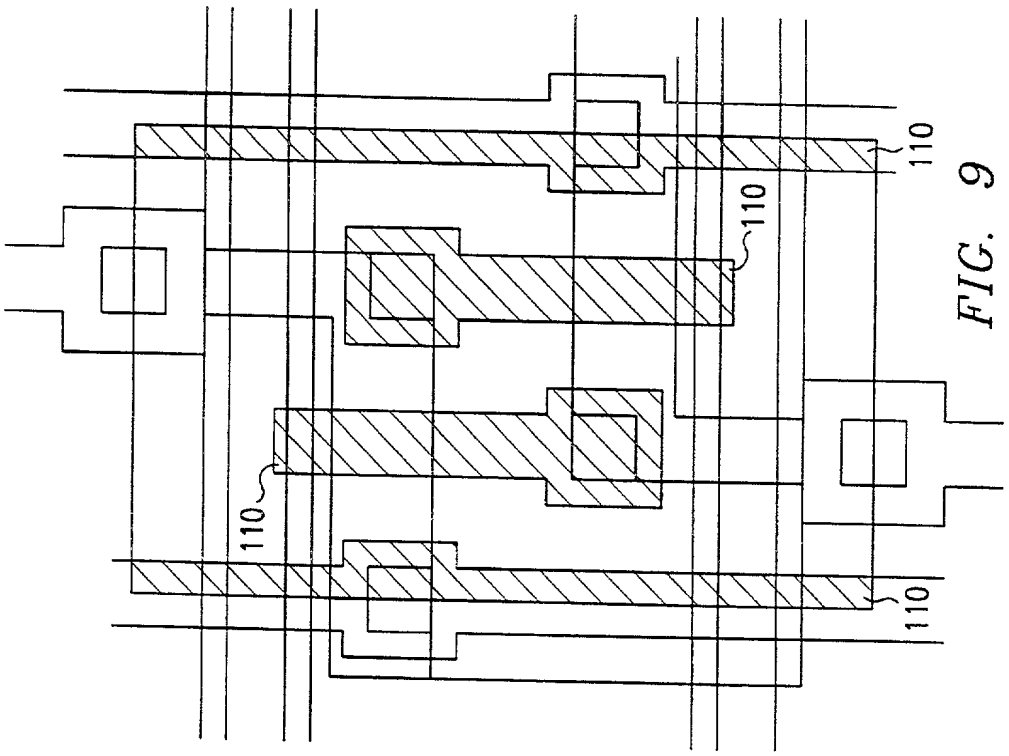


FIG. 9

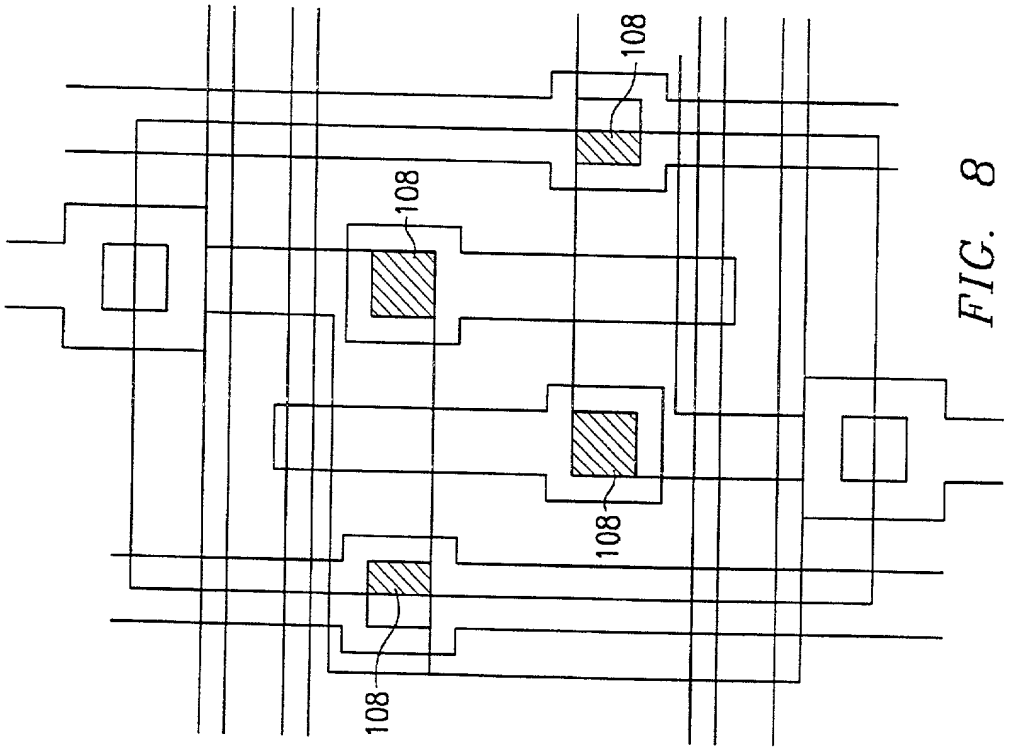


FIG. 8

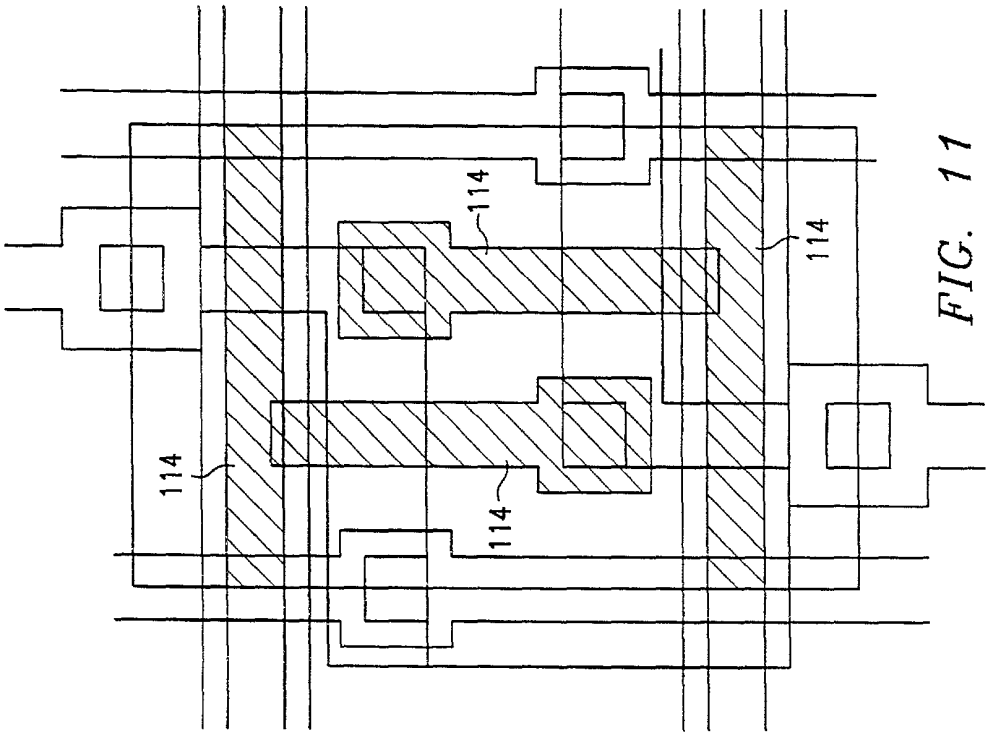


FIG. 11

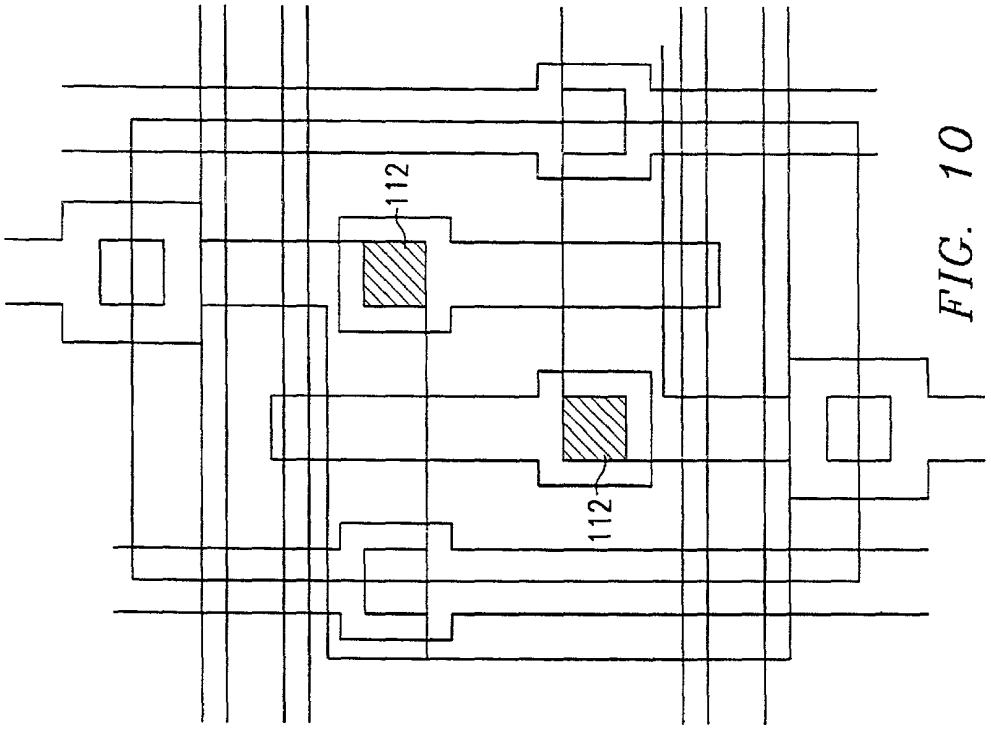


FIG. 10

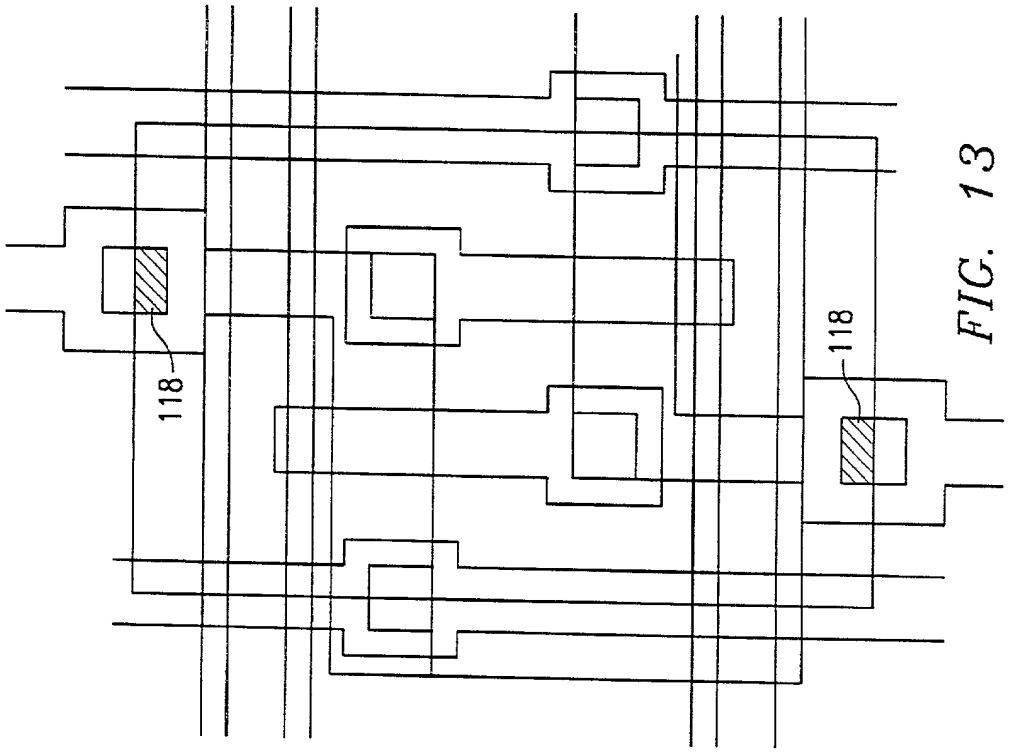


FIG. 13

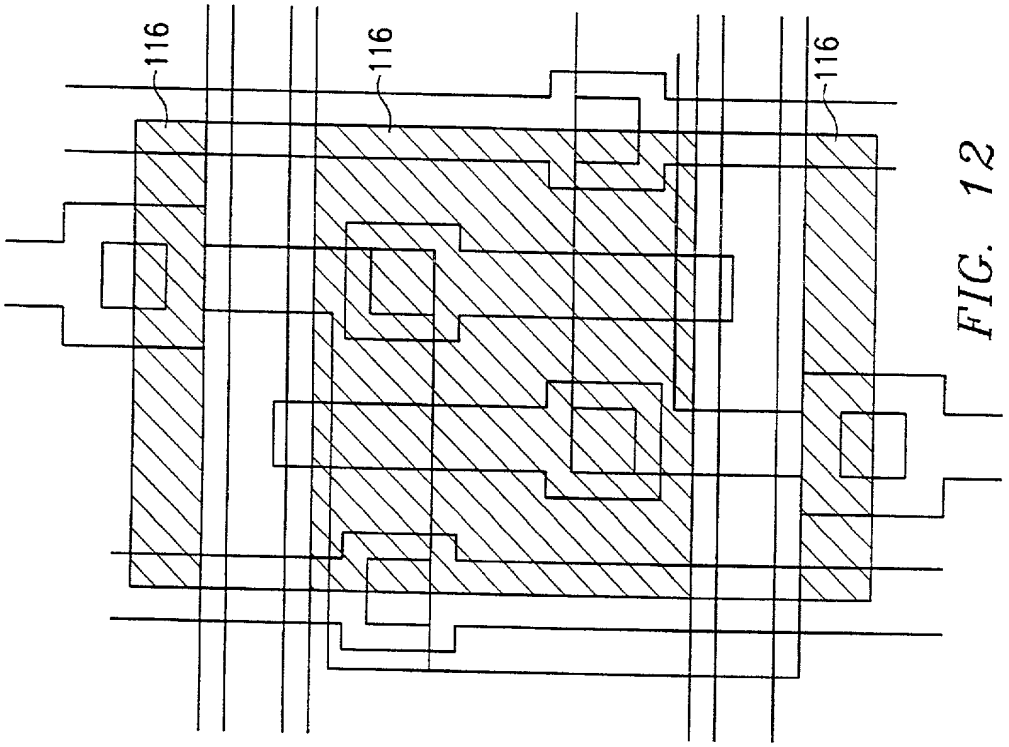


FIG. 12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentees: Frank Randolph Bryant
Tsiu Chiu Chan

Patent No.: 5,825,070

Title: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

Issued: October 20, 1998

Atty Dk No.: 96-C-126

Reissue Application

Applicants: Frank Randolph Bryant
Tsiu Chiu Chan

Serial No.:

Title: STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

Filing Date: October 20, 2000

Atty Dk No.: 96-C-126RE (1678-31)

FIRST REISSUE APPLICATION DECLARATION BY THE INVENTOR

As a below named inventor, I hereby declare:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter that is claimed in patent number 5,825,070, granted October 20, 1998, and for which a reissue patent is sought on the invention entitled:

STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

the specification of which

☑ is attached hereto.

☐ was filed on _____ as reissue application number _____ and was amended on _____ (if applicable). If the filing date, amendment date, or reissue application number are not included when I execute this Declaration, I authorize the below appointed attorney(s) and/or agents(s) to insert the filing date, amendment date, or reissue application number when they become available.

I have reviewed and understand the contents of the above–identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all that apply.)

☑ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming less than he had the right to claim in the patent.

☐ by reason of other errors.

Errors upon which reissue is based are described as follows:

The equation in column 4 and claims 4 and 9 of the '070 patent contains a typographical error. Specifically, the last term of the equation is inverted. Therefore, I have corrected each occurrence of this equation.

In claim 1, I have replaced "a product of the first width and the first thickness is greater than or equal to a product of the second width and the second thickness" with "a product of the second width and the first thickness is greater than or equal to a product of the first width and the second thickness" to broaden the scope of protection that the '070 patent affords my invention.

In claim 6, I have replaced "a product of the second width and the second thickness is greater than or equal to a product of the first width and the first thickness" with "a product of the first width and the second thickness is greater than a product of the second width and the first thickness" to broaden the scope of protection that the '070 patent affords my invention.

Because one can describe an aspect of my invention in terms of a gate insulator other than an oxide, I believe that the lack of claims directed to this feature unduly limits the scope of protection that the '070 patent provides to my invention. Therefore, I have added new circuit claims 13 – 20 and new memory-cell claims 21 – 22.

All errors corrected in this reissue application arose without any deceptive intention on my part.

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: LISA K. JORGENSON, Reg. No. 34,845; THEODORE E. GALANTHAY, Reg. No. 24,122; ROBERT D. MCCUTCHEON, Reg. No. 38,717; MARIO DONATO, Reg. No. 37,816; and all attorneys associated with Customer Number 000996.

Correspondence Address: Direct all communications about the application to:

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Carrollton, Texas 75006-5039
Phone: (972) 466-6000
Fax: (972) 466-7044

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or made the subject of an inventor's certificate issued prior to the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country more than one year prior to the filing date of the original U.S. application.

I do not know and do not believe that the claimed invention was ever in public use or on sale in the United States of America more than one year prior to the filing date of the original U.S. application.

I hereby claim the benefit of priority, under 35 U.S.C. § 119 and 35 U.S.C. § 120, of any foreign application(s) for patent or inventor's certificate on which priority was claimed in the above-identified issued patent.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon, or any patent to which this declaration is directed.

Frank Randolph Bryant _____ _____
Full Name of Inventor — Citizenship

_____
Residence

_____
Post Office Address (if different from Residence)

_____ _____
Inventor's Signature — Date

Tsiu Chiu Chan _____ _____
Full Name of Inventor — Citizenship

_____
Residence

_____
Post Office Address (if different from Residence)

_____ _____
Inventor's Signature — Date